



6th Workshop on Design Automation for Understanding Hardware Designs DUHDe 2019

Friday, March 29, 2019, Florence, Italy (DATE Friday Workshop)

<https://duhde2019.ict.tuwien.ac.at>

Understanding a hardware design can be a tough process. When entering a large team as a new member, when extending a legacy design, or when documenting a new design, a lack in understanding the details of a design is a major obstacle for productivity. In software engineering, topics like software maintenance, software understanding or reverse engineering are well established in the research community and partially tackled by tools. In the hardware area, the re-use of IP-blocks, the growing size of designs and design teams leads to similar problems. Understanding of hardware requires deep insight into concurrently operating units, optimizations to reduce the required area, and specially tailored functional units for a particular use. In hardware security, it is vital to verify properties for security-critical paths of a design, which includes to fully understand a design pre- and post-synthesis.

The workshop focus includes but is not limited to the following topics in design understanding:

- Design descriptions from the formal specification level (FSL) to electronic system level(ESL) down to register transfer level (RTL)
- Extraction of high-level properties
- Knowledge extraction from design structures at any level of abstraction
- Feature localization: Localization of code implementing specialized functionality
- Data/Control path extraction
- Reverse engineering
- Innovative GUIs for design and verification
- Analysis of interaction between hardware and software
- Metrics for (open-source) intellectual property (IP) cores
- Formal methods for design understanding
- Machine learning for design understanding
- Future applications of design understanding

Submissions may be extended abstracts of 2 pages or full papers of 6 pages in IEEE or ACM conference style. Informal proceedings will be distributed electronically. Please submit your contributions at: <https://www.softconf.com/date19/DUHDe>

Submission deadline (extended): Dec. 17, 2018; Notification: Jan. 21, 2018; **Final version:** Feb. 28, 2019

Technical program committee

Maciej Ciesielski, University of Massachusetts, USA
Azadeh Davoodi, University of Wisconsin Madison, USA
Görschwin Fey, Hamburg University of Technology Germany
Tara Ghasempouri, Tallinn University of Technology, Estonia
Ian Harris, University of California Irvine, USA
Jan Malburg, German Aerospace Center, Germany
Heinz Riener, EPFL, Switzerland
Jannis Stoppe, DFKI GmbH, Germany
Pramod Subramanyan, Indian Institute of Technology Kanpur, India
Georg Weissenbacher, Vienna University of Technology, Austria
Clifford Wolf, SymbioticEDA, Austria
Cunxi Yu, EPFL, Switzerland

Organization

Christian Krieg, Vienna University of Technology (TU Wien), Austria, christian.krieg@tuwien.ac.at
Oliver Keszöcze, Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany, oliver.keszoecze@fau.de